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A Surface Tailoring Method of Ultrathin Polymer Gate Dielectrics for Organic Transistors: Improved Device Performance and the Thermal Stability Thereof

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Tailoring the surface of the dielectric layer is of critical importance to form a good interface with the following channel layer for organic thin film transistors (OTFTs). Here, a simple surface treatment method is applied onto an ultrathin (<15 nm) organosilicon-based dielectric layer via the initiated chemical vapor deposition (iCVD) to make it compatible with organic semiconductors without degrading its insulating property. A molecular-thin oxide capping layer is formed on a 15 nm thick poly(1,3,5-trimetyl-1,3,5-trivinyl cyclotrisiloxane) (pV3D3) by a brief oxygen plasma treatment. The capping layer greatly enhances the thermal stability of the dielectrics, without degrading the original mechanical flexibility and insulating performance of the dielectrics. Moreover, the surface silanol functionalities formed by the plasma treatment can also be utilized for the surface modification with silane compounds. The surface-modified dielectrics are applied to fabricate low-voltage operating (<5 V) pentacene-based OTFTs. The highest field-effect mobility of the device with the surface-treated 15 nm thick pV3D3 is 0.59 $cm^2 V^{-1} s^{-1}$, which is improved up to two times compared to the TFT with the pristine pV3D3. It is believed that the simple surface treatment method can widely extend the applicability of the highly robust, ultrathin, and flexible pV3D3 gate dielectrics to design the surface of the dielectrics to match well various kinds of organic semiconductors.

1. Introduction

Organic thin film transistors (OTFTs) have drawn a considerable research interest due to their unique advantages including cost-effectiveness, low process temperature suitable for flexible substrates, mechanical flexibility, and lightweight. In last decade, to harness these benefits of OTFTs, various kinds of electronic devices (e.g., displays, sensors, radio frequency identification (RFID) tags) had been fabricated using OTFTs.[1,2] For further extended application of OTFTs to low-power-consuming and portable devices, the device performance must be substantially improved. To this end, high-performance organic gate dielectric layers with high mechanical stability and large-area processability are urgently requested.[1]

However, OTFTs made of polymer gate dielectrics are suffering from high operating voltage, typically exceeding 20 V,[3,4] due to the gate dielectrics with the thickness often greater than 100 nm to ensure low gate leakage current.[4] Thermally crosslinked polymers including poly(4-vinylphenol) (PVP),[5] Cytop,[6] benzocyclobutene (BCB),[7] and polyimides (PIs)[8] have been adopted for gate dielectrics, but only few of them could successfully reduce the operating voltage of OTFTs down to 10 V by reducing the thickness of dielectric layer. Moreover, the high annealing temperature required to induce the crosslinking of polymer gate dielectrics is also problematic, which may cause damage to OTFTs and limit their application to thermally vulnerable substrates.

Besides reducing the operating voltage of OTFTs, controlling the interface between dielectric and semiconductor is another critical factor to optimize the performance of OTFTs.[9,10] Applying self-assembled monolayers (SAMs)[10] or plasma treatment[11] had been widely applied to optimize the film morphology of semiconductors on the surface of gate dielectrics. However, most of these SAM treatment procedures require specific surface coupling reaction, and had been applied mostly onto inorganic dielectric layers rather than polymer dielectrics, mostly due to the lack of target surface functionalities on most of the polymer dielectrics and/or a reliable, damage-free coupling reaction applicable onto the polymer dielectrics.

Recently, we have proposed initiated chemical vapor deposition (iCVD) as a new deposition method to form ultrathin (<10 nm) crosslinked polymer dielectrics with high density.[12] iCVD is a well-established dry process, which can deposit highly pure polymer thin films in mild process temperature (10–40 °C) and pressure (in the order of 100 mTorr).[13] Especially, an organosilicon polymer, poly(1,3,5-trivinyl-1,3,5-trimethyl cyclotrisiloxane) (pV3D3), exhibited an extremely low leakage current (less than 10^{-9} A cm^{-2} at 3 MV cm^{-1}) even with ultralow thickness (≈6 nm), and chemical/mechanical robustness. Nevertheless,

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surface modification of such a thin layer of pV3D3 to tailor the interface for various semiconductors has not yet been demonstrated so far.

Here, we formed a molecular thin SiO_x capping layer on the top of 15 nm thick pV3D3 dielectrics by introducing a simple oxygen plasma treatment to modify the surface of pV3D3. It is well known that oxygen plasma treatment or ultraviolet/ozone (UVO) irradiation can produce SiO_x skin layers on crosslinked polysiloxanes,[14] and the same approach was also applicable to the organosilicon pV3D3 films. The insulating property of O_2 plasma-treated pV3D3 was maintained even after the thermal exposure of 280 °C up to 3.5 h in ambient air, confirming the improved thermal and environmental stability of ultrathin pV3D3 dielectrics. Furthermore, the O_2 plasma-treated pV3D3 thin film exhibited high flexibility up to tensile strain of 3.3%, which is far superior than previously reported SAM/AlO*x*-based dielectric layer, whose yield strain was 1.5%.[15]

The surface silanol (—Si—OH) groups formed by the plasma treatment on the SiO_x capping layer could further be utilized for the purpose of surface modification platform using silane-based SAM treatment. Various kinds of silane compounds could successfully change the surface characteristics of pV3D3 dielectric layer. The exquisite tunability of surface functionality could further be harnessed to optimize the interfacial compatibility with the following channel layer. As an example, pentacene-based OTFTs with various kinds of silane-treated pV3D3 were fabricated and a substantial improvement of OTFT performance was achieved. The simple, but versatile method to form oxide capping layer could significantly improve the device performance by controlling the surface functionality, as well as increasing the thermal stability of the ultrathin pV3D3 dielectric layer.

2. Results and Discussion

A vapor-phase polymerization method, iCVD was used for the deposition of pV3D3 and a densely crosslinked polymer film was formed, as illustrated in Figure S1 (Supporting Information). pV3D3 is composed of core hexagonal Si—O rings surrounded by aliphatic carbon backbone chains. Because the pV3D3 is composed of Si—O rings, a brief O_2 plasma exposure (50 W for 15 s) (**Figure 1**a-i) can efficiently remove the surface carbon components in pV3D3 layer to leave a thin SiO_x capping layer on pV3D3. Especially, the top surface of SiO_x capping layer consists of hydrophilic silanol groups (Si—OH), which can serve as reactive sites with silazanes and silanes to form a stable Si—O—Si linkage (Figure 1 a-ii).[16] This silanol coupling reaction can further be used as a tool for surface modification of pV3D3 dielectric layer. Unlike the most of carbon-based polymer dielectrics where the same silane treatment will only form an unstable Si—O—C bonding, silane treatment on

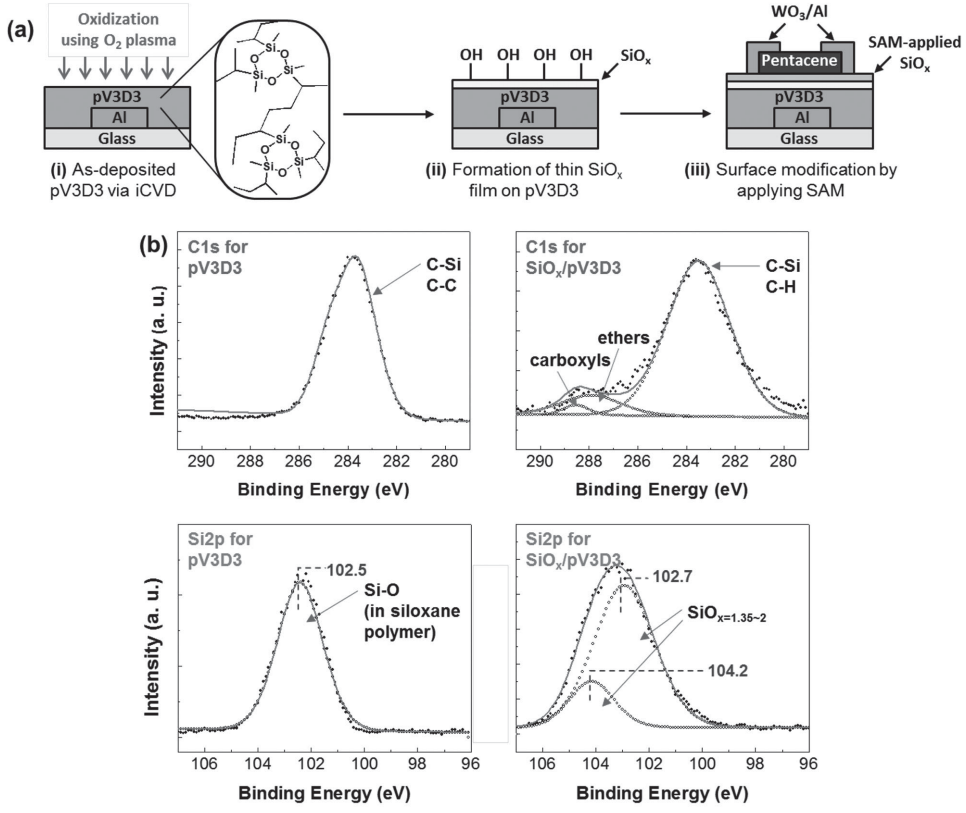

Figure 1. a) Schematic of the preparation steps of surface-modified pV3D3 dielectric layers. i) and ii) indicates the formation of nanometer-thick oxide capping layer with surface silanol (—Si—OH) functionalities via O_2 plasma treatment. iii) Modified pV3D3 dielectric layer with various SAM materials including HMDS, OTS, and PFTS are applied to fabricate pentacene TFTs. b) High-resolution XPS spectra of C1s (top) and Si2p (bottom) for untreated (left) and O_2 plasma-treated (right) pV3D3, respectively.

plasma-treated pV3D3 can modify the surface using SAM with highly reliable Si—O—Si linkage. The SAM materials used in this work to tailor the surface of pV3D3 dielectrics were hexamethyldisilazane (HMDS),[10] octadecyltrimethoxysilane (OTS),[17] and trichloro(1*H*, 1*H*, 2*H*, 2*H*-pefluorooctyl)silane (PFTS),[18] which are most commonly chosen reagents for the surface treatment of gate dielectrics, especially in pentacene-based TFTs on well-established SiO_2 dielectric layer (Figure 1a-iii).[19]

First, X-ray photoelectron spectroscopy (XPS) was performed to explore the surface components of plasma-treated pV3D3. The XPS survey scans and high-resolution scans of C1s and Si2p spectra for the pV3D3 before and after the plasma treatment were compared, as shown in Figure 1b and Figure S2 (Supporting Information). The XPS survey and high-resolution C1s scan indicate that the pristine pV3D3 contains considerable amount of carbon in C—Si and C—C bonds. On the other hand, after the plasma treatment, overall surface composition of C was significantly reduced (Figure S2, Supporting Information) and the peaks related to the oxidized carbons were newly emerged (Figure 1b, top right). In particular, the Si—O peak in Si2p XPS spectra of untreated pV3D3 was slightly shifted to the higher binding energy after the plasma treatment (Figure 1b, bottom). The continuous shift of the main peak towards higher binding energies indicates the increase of O content in the SiO_x layer.[20]

Atomic force microscopy (AFM) images and XPS depth profiles of the pristine and O_2 plasma-treated pV3D3 are also shown in **Figure 2**. The surface became hydrophilic instantly after the plasma treatment, but the surface roughness and topography remained unchanged apparently even after the O_2 plasma treatment (Figure 2a,b). This observation indicates that the plasma treatment condition applied in this work was gentle enough not to cause any crack or winkle on the dielectric surface, which could originate from the difference in the elastic modulus between the formed SiO_x skin layer and the pV3D3 layer underneath.[21] In the XPS depth profiling in Figure 2c, concentrations of Si, C, and O were constant along the perpendicular direction. This confirms the uniform composition of pV3D3 formed via the iCVD process, which is fully consistent with the previous observation.[12] On the other hand, unlike the untreated pV3D3, surface of O_2 plasma-treated pV3D3 showed significantly increased O concentration up to 60% and lowered C concentration of 11.8%, as shown in Figure 2d, illustrating the selective etching of carbon components in pV3D3 layer by the applied oxygen plasma. The sharp change of C and O concentration near the surface indicates that the oxidation of pV3D3 by the oxygen plasma is strictly confined only to the very surface layer. The concentration of Si remained almost constant throughout the depth profile, indicating that the plasma oxidation process did not etch the Si component out, unlike the case of C. A slight increase at the surface of Si concentration was observed at the skin oxide layers, most likely due to the relatively heavy etching of C component to form SiO_x layer. The estimated thickness of SiO_x layer on pV3D3 by the XPS depth profiling was no larger than 3 nm, which matches well with the optically measured thickness obtained from ellipsometry (data not shown).

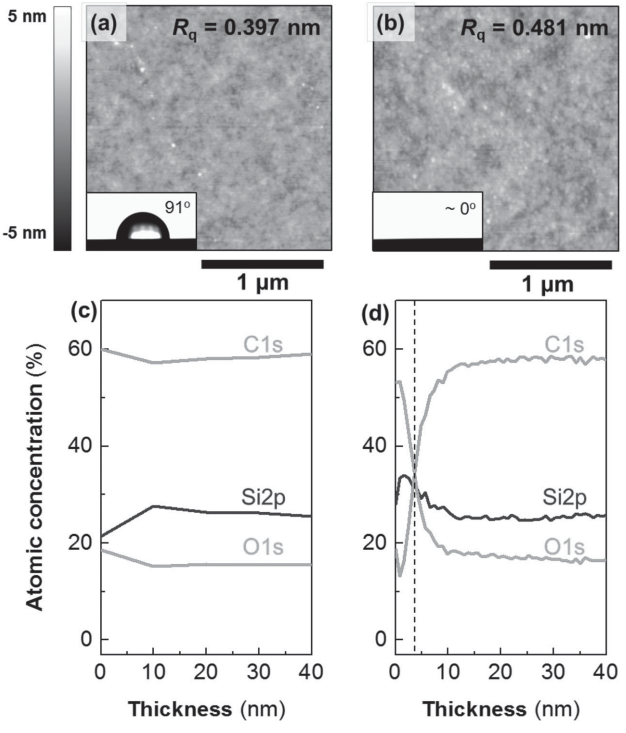

Figure 2. AFM images of a) untreated and b) O_2 plasma-treated pV3D3 surfaces. Inset images indicate the water contact angle of each surface. Root-mean-square roughness (R_q) of each surface was also noted in the image. The XPS depth profiling of c) untreated and d) O_2 plasma-treated pV3D3, respectively.

To monitor the effect of O_2 plasma treatment on pV3D3 to the insulating properties of pV3D3 dielectrics, a metal-insulator-metal (MIM) device was fabricated with O_2 plasma-treated 15 nm thick pV3D3 layer. The leakage current density (J) of O_2 plasma-treated pV3D3 film was lower than 3×10^{-9} A cm^{-2} in a range of ± 3 MV cm^{-1}, confirming that the plasma treatment did not damage the insulating property of bulk pV3D3 film (in **Figure 3**a). The insulating properties of various SAM-treated pV3D3 layers were also monitored using MIM devices with 15 nm thick pV3D3 layers whose surfaces were modified with HMDS, OTS, and PFTS. Even with the extremely thin dielectrics, the low J of pV3D3 was unchanged after the HMDS, OTS, and PFTS treatment (Figure 3b), which clearly indicates that the 15 nm thick pV3D3 is thermally and chemically robust enough to withstand the SAM treatment procedure requiring up to 150 °C of annealing temperature. The surface modification of pV3D3 dielectric layer with the SAM layers was confirmed by water contact angle (WCA) analysis. The WCA of bare pV3D3 layer changed from 91° to 71°, 95°, and 106° after treating with HMDS, OTS, and PFTS, respectively (in the inset figure in Figure S3, Supporting Information). The surface roughnesses of modified layers were also sufficiently low (root-mean square (RMS) roughness (R_q) of < 0.4 nm), as shown in the AFM images in Figure S3 (Supporting Information). Furthermore, the pV3D3 film retained its own flexibility after the plasma treatment, which can be seen in Figure 3c. Both of the MIMs on polyethylene naphthalate (PEN) substrates fabricated with as-deposited and plasma-treated pV3D3 thin film exhibited virtually unchanged J upon to a radius of curvature (R) as small as 1.5 mm for a tensile stress, which corresponds to a tensile strain of 3.3%.

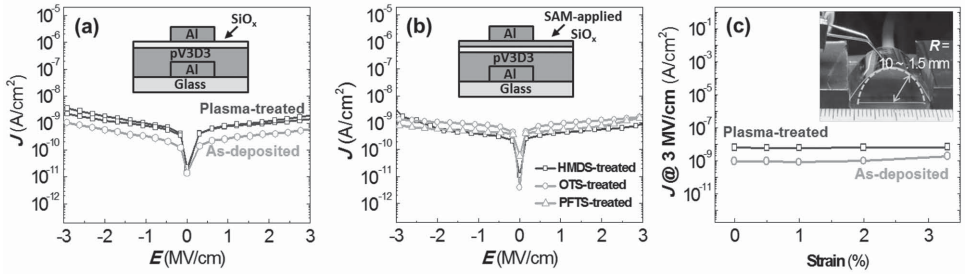

Figure 3. a) Leakage current density (J) vs electric field (E) of as-deposited and plasma-treated 15 nm thick pV3D3. b) J vs E characteristics of MIM devices with 15 nm thick pV3D3 dielectric layers modified with various SAMs of HMDS, OTS, and PFTS. c) The J measured at 3 MV cm^{-1} for various tensile strain values for as-deposited and plasma-treated 30 nm thick pV3D3. The inset photographs show the set-ups for bending test of MIM devices.

To investigate the long-term thermal stability of plasma-treated pV3D3 layer, the layer was exposed to the temperature of 280 °C. The J of MIM devices with plasma-treated pV3D3 layer was as low as 2×10^{-8} A cm^{-2} at 3 MV cm^{-1} even after a 3.5-hr thermal annealing at 280 °C (in **Figure 4**b), which suggests the plasma-treated layer is thermally stable enough to withstand further surface modification process with SAMs. The improved thermal stability is likely originated from the existence of robust oxide skin layer, which could substantially stabilize the chain movement of unconverted pV3D3 layer underneath the oxide skin layer.[22] For comparison, thermal stability of the pristine pV3D3 layer was investigated with the same thermal treatment condition applied above. With the lapse of exposure time, the insulating property of pV3D3 was severely

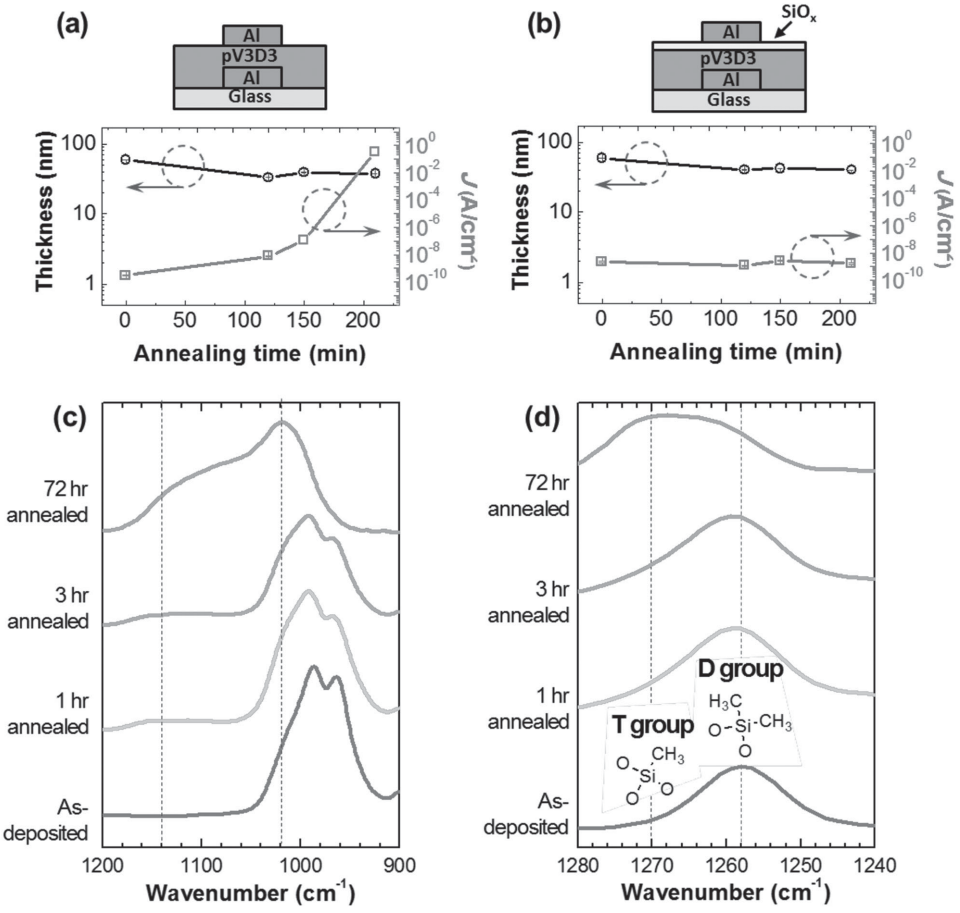

Figure 4. Change of thickness with the increased of annealing time with a temperature of 280 °C. a) as-deposited pV3D3 and b) plasma-treated pV3D3 with SiO_x capping layer. c) FTIR spectra of as-deposited pV3D3 and films annealed at 150 °C for 1, 3, and 72 h in the range showing the Si—O—Si stretching vibration. Broadening and peak shift from 900–1050 cm^{-1} to 1000–1200 cm^{-1} indicates the ring opening event of pV3D3. d) FT-IR spectra of as-deposited pV3D3 and films annealed at 150 °C for 1, 3, and 72 h for the Si—CH_3 bonding region. Peaks at 1260 and 1270 cm^{-1} correspond to $O_2Si(CH_3)_2$ (D-group) and $O_3Si(CH_3)$ (T-group), respectively. Formation of T-group means a crosslinking structure was emerged, in which silicon is bound to three network-forming oxygen atoms.

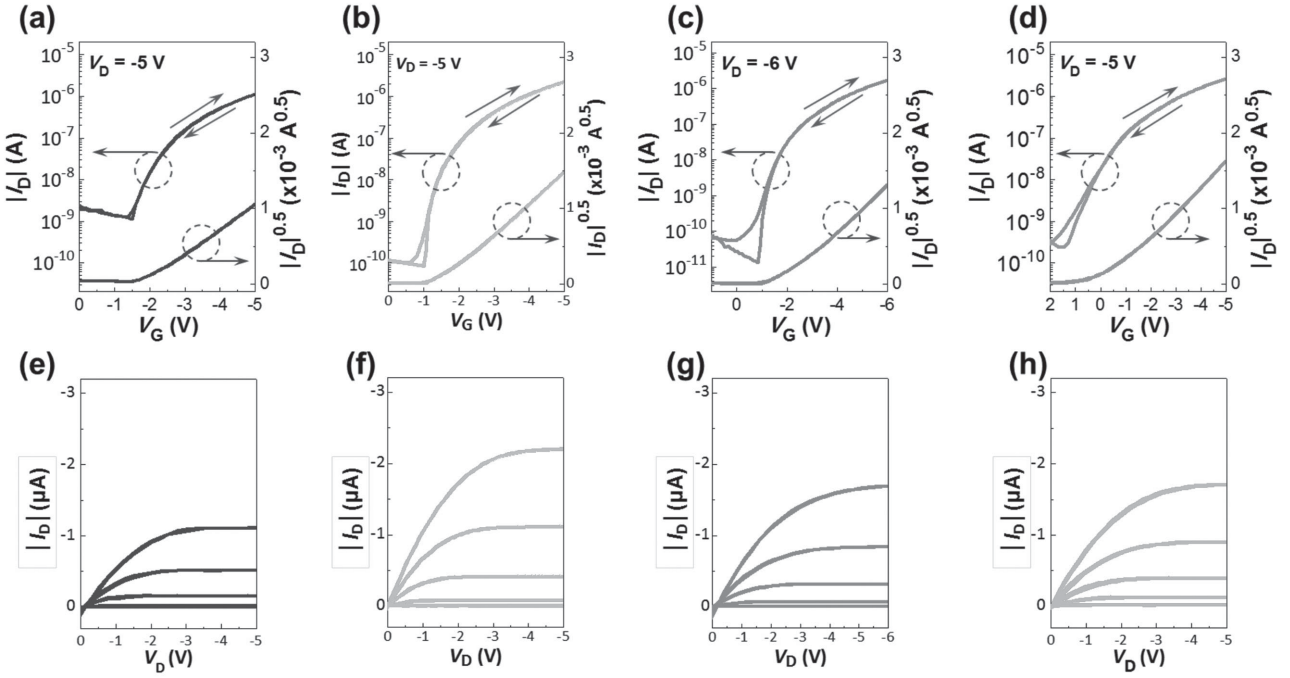

Figure 5. a–d) Transfer and e–h) output characteristics of pentacene TFTs fabricated with pV3D3 and SAM-treated pV3D3 as a dielectric layer: a,e) untreated, b,f) HMDS-treated, c,g) OTS-treated, and d,h) PFTS-treated pV3D3, respectively.

degraded (Figure 4a). Note that no noticeable loss of film thickness was detected from the both of thermally annealed pristine and plasma-treated pV3D3 layer (Figure 4a,b), which is fully consistent with the thermogravimetic analysis (TGA) of pV3D3 in Figure S4 (Supporting Information), indicating no major mass loss in bulk of pV3D3 up to 280 °C. However, damage to the bulk pV3D3 film with a thermal stress above 280 °C was unavoidable even with the plasma-treated pV3D3 layer, due to the severe mass loss above this temperature, as shown in Figure S4 (Supporting Information).

To figure out the reason why the insulating property was degraded without the mass loss, Fourier transform infrared (FTIR) analysis of as-deposited pV3D3 and thermally annealed pV3D3 films with several thermal stress time intervals at 150 °C was performed. Figure 4c demonstrates the evolution of the Si—O bonding nature of the annealed pV3D3 films. The thermal annealing for more than 1 h induced an increase of the peak intensity at the 1140 cm^{-1} in the FTIR spectrum. The evolution of the FTIR peak shape for the thermally annealed pV3D3 layer in this wavenumber is quite similar to that of change in linear polysiloxane, such as polydimethylsiloxane (PDMS), which strongly infers that the breakage of siloxane ring in pV3D3 was occurred to form linear siloxane by the applied thermal stress.

Further increase of the annealing time up to 72 h resulted in a large peak shift in the FTIR spectra, featured by the formation of a broad peak at around 1140 cm^{-1} and the shift of major peak from 950–1000 to 1020 cm^{-1} (Figure 4c). The broad peak around 1000–1200 cm^{-1} and the peak at 1020 cm^{-1} indicate the formation of a silsesquioxane (SQ)-like cage structure[23] and suboxide (—O—Si—O—)Si— structure,[24] respectively, illustrating that the siloxane ring structure in pV3D3 layer was damaged to form a suboxide inorganic layer.[25] The formation of cage and suboxide structure in pV3D3 film is most likely due to the reaction between oxygen and reactive sites in the linearized pV3D3 by the thermal damage. Dramatic change was also found in Si—CH_3 bonding peak of the pV3D3 film annealed for 72 h (Figure 4d). The peaks near the 1260 and 1270 cm^{-1} correspond to Si—CH_3 bending mode in $O_2Si(CH_3)_2$ (D-group) and C—H_3 bending mode in $O_3Si(CH_3)$ (T-group), respectively.[26] D-group linkage is dominant in as-deposited pV3D3. As the annealing time increased up to 72 h, a significant fraction of the silicon bound in D-group in the as-deposited polymer was converted to T-group, which also strongly supports the aforementioned observation of SQ-like cage structure in the annealed pV3D3 film.

Finally, the pV3D3 thin layers whose surface was modified with HMDS, OTS, and PFTS were adopted as dielectric layers for the fabrication of pentacene TFTs. **Figure 5** shows the device performance of the pentacene TFTs with HMDS, OTS, and PFTS-treated pV3D3 as gate dielectric layers, respectively. A pentacene TFT with pristine pV3D3 layer was also fabricated as a control device. All the relevant electrical parameters extracted from the graphs in Figure 5 were summarized in **Table 1**. The OTFT with HMDS-treated pV3D3 in Figure 5b showed a significantly lowered threshold voltage (V_T) close to zero, and an improved on-off ratio of >10^5, far larger than that of control pentacene TFT (Figure 5a). The field-effect mobility (μ_{FET}) of device with HMDS surface treatment was reached up to 0.59 cm^2 V^{-1} s^{-1}, which was improved up to two times compared to the mobility of the pentacene TFT with pristine pV3D3 dielectric layer (0.33 cm^2 V^{-1} s^{-1}). Furthermore, the subthreshold swing (*S.S.*) of the device with HMDS-treated pV3D3 was also improved to 0.216 V/decade. The on–off ratio, V_T, and *S.S.* of the OTFT with OTS-modified pV3D3 were also

Table 1. Statistical data of fabricated TFT devices.

Dielectric	Water contact angle [°]	Total thickness (T_i)* [nm]	Capacitance (C_i)* [nF cm^{-2}]	On–off ratio (I_{on}/I_{off})	Threshold voltage (V_T)* [V]	Field-effect mobility (μ_{FET})* [cm^2 V^{-1} s^{-1}]	Subthreshold swing (*S. S.*)*[V/decade]
As-deposited pV3D3	91	12.1 ± 0.2	161.5 ± 3.0	>10^3	−1.5 ± 0.01	0.33 ± 0.01	0.463 ± 0.076
HMDS-treated pV3D3	71	13.7 ± 0.2	142.3 ± 2.5	>10^4	−0.9 ± 0.01	0.59 ± 0.03	0.216 ± 0.020
OTS-treated pV3D3	95	12.3 ± 0.6	158.4 ± 7.6	>10^5	−0.2 ± 0.06	0.31 ± 0.01	0.350 ± 0.011
PFTS-treated pV3D3	106	13.0 ± 0.3	150.4 ± 3.5	>10^4	1.1 ± 0.29	0.44 ± 0.03	0.646 ± 0.069

*5 TFTs in the substrate were measured for the statistical analysis.

substantially improved, compared to the performance of the device with pristine pV3D3.

The μ_{FET} and other device performances of the OTFTs were highly dependent upon the surface morphology of the pentacene deposited on the SAM-treated pV3D3 layers.[9,10,19] To investigate the reason why the substantial improvement in device performance was achieved by the surface treatment, 3 nm thick (corresponds to 2 monolayers (MLs) of pentacene), 15 nm thick, and 40 nm thick pentacene grains on each surface was analyzed via AFM (in **Figure 6**a–d). On the hydrophobic as-deposited pV3D3 surface, a small, faceted pentacene seed layer was formed (Figure 6a, top). The small seed layer resulted in the final grain of pentacene on the as-deposited pV3D3 with the average grain size of about 100 nm. On the contrary, the surface modification of pV3D3 layer led to a drastic morphological change on the pentacene film. A layered pentacene grain structure was clearly exhibited with the average grain size of 1 μm on a slightly more hydrophilic HMDS-treated pV3D3 (water contact angle of 71°) due to the large, faceted seed layer with high surface coverage. Unlike the case of HMDS-treated pV3D3, seed layers with dendritic island-like morphology were found on the OTS-treated surface. The dendritic morphology is reported to represent a divergent polycrystalline growth initiated from a common nucleation points.[27] Because of the morphological complexity of the dendrite, the pentacene layer will have a higher chance to form intra-grain boundaries within the island domains,[28] which can explain why the OTS-treated TFTs displayed the lowest mobility among the devices. This observation is also well consistent with the previous reports on the SAM-treated SiO_2 dielectrics, where the seed layer and the resultant grain size of semiconductor were closely related with the device performance in that the increased number of grain boundaries can cause a decrease of

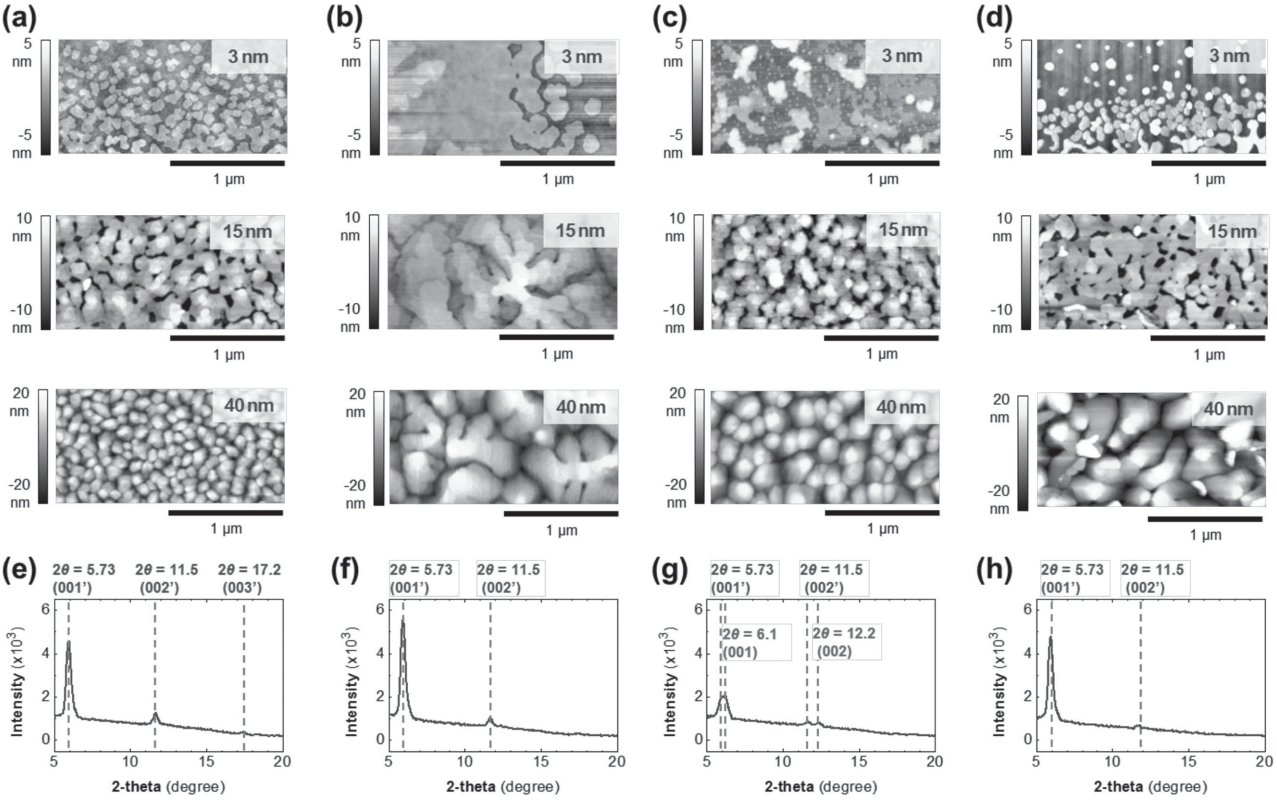

Figure 6. AFM images of thermally evaporated pentacene films (3 to 50 nm) on different dielectric surfaces: a) as-deposited, b) HMDS-treated, c) OTS-treated, and d) PFTS-treated pV3D3. (e) to (h) are corresponding XRD spectra of 40 nm thick pentacene on each surface.

mobility because the grain boundaries will act as trap sites in charge transport.[29]

Furthermore, XRD spectra of 40 nm thick pentacene on each surface were also obtained (Figure 6e–h) to further elucidate the change of device performance by the SAM treatment on pV3D3. From all pentacene layers, a series of (00*k*′) XRD patterns was detected, indicating a highly textured phase, which is called as a "thin film phase." Forming the "thin film phase" is highly advantageous to the charge transport in pentacene.[30] The intensity of (001′) lines also reflects the amount of "thin film phase" in pentacene crystal. The highest intensity was observed for the pentacene on HMDS-treated surface, while the OTS-treated surface exhibited the lowest intensity. In addition, the (00*k*) XRD patterns are observed from the pentacene layer on OTS-treated surface, which is a second phase of the pentacene, called as a "triclinic crystal bulk phase."[30] The series of (00*k*) XRD patterns only observed in OTS-treated pV3D3 indicates the disordered crystalline structure in the pentacene grain, which will negatively affect to the charge transport in pentacene.

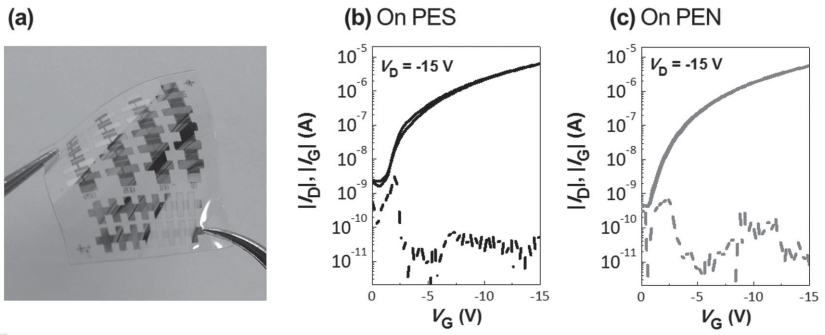

Figure 7. Pentacene TFTs on flexible substrates fabricated with HMDS-treated pV3D3 as a dielectric layer: a) digital camera image of TFTs on PES, transfer characteristics of TFTs b) on PES, and c) on PEN.

In the case of TFT with PFTS-treated pV3D3 (in Figure 5d), the on–off ratio, *S.S.*, and μ_{FET} were also improved from the device with pristine pV3D3. The seed layer of pentacene on the PFTS-treated pV3D3 was smaller than that on OTS-treated pV3D3, but compared to the morphology of the 15 nm thick pentacene films on OTS-treated surfaces, where the pentacene started forming smaller grains, more uniform pentacene layers were formed on PFTS-treated pV3D3, leading to a huge difference in final pentacene grains and further affecting to the device performance. It is worthy of noting that a significant V_T shift was observed from the device with PFTS-treated pV3D3. Previous report indicated that SAMs with fluorine are known to accumulate holes in the transistor channel, which can explain the shifted V_T in TFT with PFTS-treated pV3D3 dielectric layer.[18,31] The enhanced TFT performance through the SAM treatment clearly demonstrates that the pV3D3 with SiO_x capping layer can be a versatile surface modification platform. Furthermore, the achieved controllability of the surface composition of the pV3D3 layer without damaging the ultrathin dielectric layer is also essential for an optimal design of interface tailored to the semiconductors. Consequently, all OTFTs mentioned above operated with low voltage under 5 V thanks to the ultrathin gate dielectric layer. Coupled with a great advantageous characteristics of ultrathin pV3D3 dielectrics, the simple surface treatment method can be a breakthrough for next-generation electronic devices.

To fully utilize the merits of flexible gate dielectric layer as described in Figure 3c, flexible pentacene TFTs were demonstrated on polyethersulfone (PES) and PEN substrate, as shown in **Figure 7**. Here, O_2 plasma-treated 40 nm thick pV3D3 was used as a dielectric layer. HMDS was treated on the capping layer. The pentacene TFTs on flexible substrates showed analogous device performance with the devices on rigid substrates. The flexible devices exhibited V_T of lower than −1 V, μ_{FET} up to 0.45 $cm^2\ V^{-1}\ s^{-1}$, and low gate leakage current (I_G) of lower than 10^{-9} A. The surface oxidization of the pV3D3 did not damage both of dielectric layer and flexible substrate, confirming that the proposed system will enable to design flexible OTFT devices onto various kind of unconventional substrates.

3. Conclusion

In this study, a surface oxide layer was formed on the ultrathin pV3D3 using brief O_2 plasma treatment. On the pV3D3 with SiO_x capping layer, further surface modification could be achieved by use of various silicon-based coupling agents including HMDS, OTS, and PFTS, without compromising the excellent insulating property of 15 nm thick pV3D3 layer. The top SiO_x capping layer could also substantially enhance the thermal stability of pV3D3 dielectric, especially in air ambient, which is critically important to ensure the fabrication of reliable TFTs and further development of air-stable electronics including the devices for sensor applications. The TFTs with the surface-modified pV3D3 gate dielectric layer showed improved on–off ratio, and higher mobility compared to the untreated control device. The improved TFT performance is well consistent with the previous reports on the SAM-modified SiO_2 dielectric layer. Moreover, unlike the brittle inorganic dielectric layer, the ultrathin pV3D3 layer was fully compatible with various kinds of flexible substrates, thanks to the low process temperature of iCVD. Coupled with the excellent insulating property of the ultrathin pV3D3, the surface treatment method can be a powerful tool for further application to future flexible and wearable electronics.

4. Experimental Section

Substrates and Materials Preparation: All devices used in this work were fabricated on Eagle XG glass (Samsung Corning Co.) unless mentioned. Flexible TFTs were fabricated on polyethersulfone (PES, SKC Co.) and polyethylene naphthalate (PEN, Hanwha Chem.) Glasses were cleaned with ultrasonication in DI water, acetone, and isopropyl alcohol for 20 min then were dried with N_2 blowing. For PES and PEN, same cleaning steps were applied without acetone. All the chemicals used in this work were purchased from Aldrich and used as received without further purification, unless mentioned otherwise.

Depositing Poly(1,3,5-trimethyl-1,3,5-trivinyl cyclotrisiloxane) (pV3D3) via the Initiated Chemical Vapor Deposition (iCVD): 1,3,5-trimethyl-1,3,5-trivinyl cyclotrisiloxane (V3D3, Gelest, 95%) and *tert*-butyl peroxide

(TBPO) were vaporized and delivered to the iCVD reactor, which is described elsewhere. The flow rates of V3D3 and TBPO were controlled by needle valve to 2.5 and 1 sccm, respectively. The process pressure was maintained at 300 mTorr, and the filament was heated to 200 °C. Substrate temperature was maintained at 40 °C. The thickness of the deposited polymer film was controlled in situ by the interferometer.

Surface Oxidation of Organosilicon Polymer Dielectrics and SAM Surface Treatment: The surface of iCVD polymer film was briefly treated with O_2 plasma at 50 W for 15 s at the pressure of under 10^{-2} Torr. The flow rate of O_2 during the plasma treatment was maintained at 25 sccm. To modify the oxidized surface of polymer, hexamethyldisilazane (HMDS, 99.9%, Aldrich) and trichloro(1*H*,1*H*,2*H*,2*H*-perfluorooctyl)silane (PFTS, 97%, Aldrich) was spin-coated onto the substrate at 3000 rpm for 35 s. Then, the HMDS-coated and PFTS-coated substrates were annealed on a hot plate at 150 °C for 30 min and 120 min, respectively. In the case of octadecyltrimethoxysilane (OTS, 90%, Aldrich), substrates were dip coated in pure OTS for 15 s then gently washed with acetone. For the OTS-coated substrates, same annealing procedure with HMDS-coated substrates was followed.

TFT Fabrication: 50 nm thick Al for gate electrode was deposited onto Eagle XG glass by thermal evaporation with the deposition rate of 1.5 Å s^{-1}. Then, pV3D3 dielectric layer was deposited by iCVD process to the desired thickness. A SAM surface treatment was applied onto the iCVD-deposited pV3D3 layer, if necessary. On top of this layer, 50 nm of pentacene (TCI, 99.99% with sublimated grade) was thermally deposited at the base pressure of lower than 10^{-6} Torr. The deposition rate of pentacene was 0.5 Å s^{-1}. For the source and drain (S/D) electrodes, WO_3 (20 nm)/Al (30 nm) was thermally evaporated consecutively through shadow mask, producing a channel dimension of 250 μm (L) × 1000 μm (W). The base pressure for the metal layer deposition was lower than 10^{-5} Torr. All the TFT fabrication procedure was performed in a N_2-filled glove box.

Thin Film Characterization: The chemical bonds in as-deposited and thermally annealed pV3D3 films were characterized by ALPHA Fourier transform infrared (FTIR) spectrometer (Bruker, Billerica MA). Thermogravimetric data of pV3D3 film was obtained from thermogravimetric analyzer (Setsys 16/18, Setaram). The surface morphology of as-deposited pV3D3, surface-modified pV3D3, and pentacene grains were monitored with AFM (PSIA). Contact angle of the surfaces was obtained from contact angle measurement system (Phoenix Series, S. E. O. Co. Ltd.). XPS (Thermo VG scientific) analysis was also conducted to assess the surface chemical composition of the surfaces. To test the flexibility of pV3D3 and SiO*x*/pV3D3, MIM devices prepared on 100 μm thick PEN substrates in the configuration of Al (50 nm)/insulator (30 nm)/Al (50 nm) devices were bended to the direction of tensile stress. The lowest bending radius (R) for the measurement was 1.5 mm, which corresponds to a tensile strain (S) of 3.3%. The strain could be calculated from the equation below; $S = d_{sub}/(2R + d_{sub})$ where d_{sub} is the thickness of a substrate.

TFT Characterization: Capacitance (C_i) of the TFT was obtained from MIM structure with the dimension of 1 mm × 1 mm. All electrical characteristics were measured with Agilent B1500A semiconductor device analyzer. Mobility of the devices was extracted from the transconductance (g_m); $dg_m/dV_D = WL^{-1}C_i\mu$ where $g_m = \partial I_D/\partial V_G|_{VD}$.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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